REMARKS

The Examiner's Office Action mailed on April 7, 2004 has been received and its contents carefully considered.

Claims 1, 2, 4-7 and 10-13 are currently pending in this application. Claims 1, 6 and 7, which are the independent claims, are amended. New claims 14-18 are added herein.

The applicant acknowledges with appreciation the Examiner's indication that claims 6 and 7 would be allowable if rewritten or amended to overcome the rejections under 35 USC §112, second paragraph, set forth in the Office Action, and that claims 10-13 would be allowable if rewritten to overcome the rejections under 35 USC §112, second paragraph, set forth in the Office Action and also to include all of the limitations of the base claim and any intervening claims.

In the Action, claims 1, 2, 4-7 and 10-13 are rejected under 35 USC §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Specifically, with regard to claim 1, the Examiner asserts that the claimed "calculated difference signal" output from the judgment circuit does not appear to be utilized anywhere, and, the selector combines a plurality of delayed input data but does not appear to output any signals to anywhere, rendering the claim indefinite. In response, claim 1 is amended herein to specifically recite that the selector combines "the delayed input data in response to the calculated difference signal," which is calculated by the judgment circuit, and that the selector generates "as an output data, combined input data having the standard number of pixels" (new text emphasized).

With regard to claim 6, the Examiner asserts that the claimed "calculated difference" and "the delayed signal" both of which are output by the judgment circuit do not appear to be utilized anywhere in the system, again, rendering the claim indefinite. In response, claim 2 is amended to eliminate the recited "delay signal," which is unnecessary, so that the judgment circuit simply "calculates a new address value in accordance with an address value generated by the address generation circuit and the calculated difference." Further, like claim 1, claim 6 is amended to recite that the output

selector generates "as an output data, combined input data having the standard number of pixels" (new text emphasized).

With regard to claim 7, the Examiner asserts that the delayed signal output from the judgment circuit does not appear to output any signal, rendering the claim indefinite. This alleged deficiency is addressed herein by amending the characterization clause to read:

> "wherein the address generation circuit generates the write address or the read address on the basis of the address value and the delay signal calculated by the judgment circuit, and when there is a difference between the pixel number of the input data read from the memory circuit and that of the input data written in the memory circuit, some of the plural read addresses each corresponding to the plural data to be read are repeated or deleted, in accordance with the difference between the pixel numbers, the input data read from the memory circuit according to the plural read addresses constituting an output data of the video signal control circuit" (new text emphasized).

In view of the amendments to independent claims 1, 6 and 7, it is respectfully submitted that the Examiner's §112, second paragraph, rejection be withdrawn.

Claims 1, 2, 4 and 5 are again rejected in the current Action under 35 U.S.C. §103(a) as being obvious over Hickman (U.S. Patent No. 5,694,432) in view of Wang (U.S. Patent No. 5,796,796). The rejection is respectfully traversed.

The Hickman reference cited by the Examiner is directed to a digital communications system. In Hickman's digital communications system, data is transmitted with a header, so that the transmitted data includes header blocks interspersed with data blocks. The data blocks are disclosed as being of fixed length (see column 4, lines 61-67). In Hickman, the communications system monitors a count signal CNT from a FIFO counter 48 and determines whether a normal header, a long header or a short header should be added to the data by a control circuit 53 (see column 10, lines 54-59). That is, the total length of the transmitted data is regulated, and jitter thereby reduced, by adjusting the lengths of the header blocks. Hickman, however, fails to disclose "a selector combining the delayed input data in response to the calculated

difference signal to generate as an output data, combined input data having the standard number of pixels," as amended claim 1 requires. Hickman discloses no change in length of the data blocks at all.

In the Action, the Examiner notes Hickman discloses that the continuous series of data bits which occurs at the input terminal of the transmitter may consist of pixels in successive video frames (see column 21, lines 10-16). However, Hickman fails to suggest that the pixels or video signal would be processed in any manner more similar to that required by the claimed invention.

In the Action, the Examiner acknowledges that Hickman fails to disclose a delay circuit, as claim 1 requires. The Examiner relies on the Wang reference to overcome this deficiency in the disclosure of Hickman.

Wang is directed to a pointer adjustment jitter cancellation processor. Wang does disclose a plurality of delay circuits as pointed out by the Examiner (column 5, lines 48-57). However, in Wang, the delay circuits delay a compensated write clock signal (see column 5 lines 50-52), rather than "delaying the input data with a plurality of delay times so that the delay circuit outputs a plurality of delayed input data" (emphasis added), as amended claim 1 requires. The function of the delay circuits in Wang and the present invention are completely different. It is clear that the combination suggested by the Examiner is not suggested by the references considered as a whole, and even if it were, the combination of Hickman and Wang would not yield the claimed invention. Moreover, Wang, like Hickman, also fails to teach or suggest "a selector combining the delayed input data in response to the calculated difference signal to generate as an output data, combined input data having the standard number of pixels" This is an important feature of the claimed invention that the Examiner's analysis has largely ignored.

For at least the foregoing reasons, it is respectfully submitted that amended claim 1, as well as dependent claims 2, 4 and 5, patentably distinguish over the applied references, whether considered individually or in combination.

New dependent claims 14-18 are added to protect additional features of the invention disclosed in the application but not previously recited in the claims.

In summary, it is submitted that this Amendment places the application, with claims 1, 2, 4-7 and 10-18, in condition for allowance. Notice of allowance and passing of this application to issue are respectfully requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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